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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,404	07/08/2004	Che-Li Lin	12921-US-PA	4403

31561 7590 08/11/2009

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER
XIAO, KE

ART UNIT	PAPER NUMBER
2629	

NOTIFICATION DATE	DELIVERY MODE
08/11/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/710,404	LIN, CHE-LI	
	Examiner	Art Unit	
	Ke Xiao	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-12 and 15-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-12 and 15-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 15 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Jun (US 2003/0117350 A1).

Regarding **Claim 15**, Jun teaches a gate driver for use in a panel display apparatus to drive corresponding pixels, comprising:

a gate input interface, receiving the serial protocol image display signal (Jun, Fig. 1 elements 3a and 3b, Abstract) and a clock signal (Jun, Fig. 1 clock), wherein the serial protocol image display signal and the clock signal are continuously transmitted to a next one of the gate driver, and are used for decoding out a plurality of gate input signals (Jun, Fig. 1 passed from one driver to the next and decodes the output signals from the serial data paragraphs [0011-0013]); and

a state in the art gate driver respectively receiving the gate input signals (Jun, Fig. 1 paragraphs [0011-0013] gate drivers receive the signals from the serial interface and then output them to the display);

wherein, the serial protocol image display signal is at least one of red or green or blue pair signal (Jun, Fig. 1, paragraph [0013]).

Regarding **Claim 16**, Jun further teaches that the gate input interface comprises:

a decoding unit, according to the serial protocol image display signal and the clock signal, decoding into the gate input signals and exporting to the state in the art gate driver (Jun, Fig. 1 paragraph [0011-0013] clock and gate driving data are extracted by the decoding unit in order to be outputted by the gate driver); and

a switch unit, passing the serial protocol image display signal and the clock signal to the next one of the gate drivers, and coupled with the decoding unit for exporting a decoded image information and the cock signal to the state in the art gate driver (Jun, Fig. 1 paragraph [0011-0013] bypass).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, 6-8, 12, 17-26 and 30 rejected under 35 U.S.C. 103(a) as being unpatentable over Akahori (US 20050012705).

Regarding **Claims 1, 19, 23**, Akahori teaches a serial-protocol panel display system, suitable of using in a panel display apparatus (Akahori, Fig. 1), comprising:

a pixel array unit (Akahori, Fig. 1 element 100);

a plurality of gate drivers and source drivers, used for driving the pixel array unit to display image (Akahori, Fig. 1 elements 101 and 102); and

a video graphic adapter (VGA) unit, according to a serial protocol, to export a serial protocol image display signal and a clock signal to a corresponding one of the gate drivers and one of the source drivers (Akahori, Fig. 1 LCD controller takes the serial protocol and separates it into gate driving section and source driving section),

wherein the gate and source drivers respectively decode the serial protocol image display signal, so as to obtain a plurality of input signals, and to drive pixels of the pixel array unit (Akahori, Fig. 2 elements 101 and 102 respectively uses the signals that they are provided in order to drive the LCD).

Akahori fails to teach wherein the serial protocol image display signal is at least one of red or green or blue pair signal.

The examiner takes official notice that it is well known in the art at the time of the invention that display data signals can include red green and blue pair signals. It would have been obvious to one of ordinary skill in the art at the time of the invention to add red green and blue pair data to the gray data signal of Akahori in order to allow for a full color display.

Regarding **Claims 2 and 20**, Akahori further teaches a connector, coupled between the VGA unit and the gate and source drivers (Akahori, Fig. 1 connections lines between the VGA unit and the drivers).

Regarding **Claim 3 and 21**, Akahori as modified above further teaches a gamma correction unit, to provide color management information to a portion of the source drivers (Akahori, Pg. 3 paragraph [0039]).

Regarding **Claim 4 and 22**, Akahori inherently teaches a power source unit, to provide a plurality of voltage levels for use in the panel display system (Akahori inherently teaches a power supply because all displays *must* have power supplies to provide different voltages levels for the different ICs).

Regarding **Claim 6 and 24**, Akahori further teaches that each of the source drivers includes:

a source input interface, receiving the serial protocol image display signal exported from the VGA unit and the clock signal (Akahori, Fig. 10 SDC), wherein the serial protocol image display signal and the clock signal are continuously transmitted to a next one of the source drivers (Akahori, Fig. 10 SDC are shifted from one driver to another), and are used for decoding out a plurality of source input signals in the input signals (Akahori, Fig. 10 elements 901n and 903n); and

a state in the art source driver respectively receiving the source input signals (Akahori, Fig. 10 elements 901n and 904n external setting terminal).

Regarding **Claim 7 and 25**, Akahori as modified above further teaches that the source input interface comprises:

a decoding unit, according to the serial protocol image display signal and the clock signal, decoding into the source input signals and exporting to the state in the art source driver (Akahori, Fig. 10 elements 902n and 903n); and

a switch unit, passing the serial protocol image display signal and the clock signal to the next one of the source drivers, and coupled with the decoding unit for

exporting a decoded color information and the clock signal to the state in the art source driver (Akahori, Fig. 10 elements 100n).

Regarding **Claims 8 and 26**, Akahori as modified above further teaches that the serial protocol image display signal includes red, green and blue (Akahori, Fig. 1 data, and official notice).

Regarding **Claim 12 and 30**, Akahori further teaches that the VGA unit includes:

a VGA chip (Akahori, Fig. 1 element 103); and

a protocol encoder, coupled with the VGA chip for encoding, and exporting the serial protocol image display signal and clock signal (Akahori, Fig. 1 element 103 outputs SDC and horizontal sync to the source and gate drivers respectively).

Regarding **Claim 17**, Akahori teaches a video graphic adapter, suitable for use in a panel display apparatus to receive image control signals (Akahori, Fig. 1 element 103), comprising:

a VGA chip, for receiving an image control signal; and a protocol encoder, coupled with the VGA chip for encoding, and exporting a serial protocol image display signal and a clock signal (Akahori, Fig. 1 element 103 outputs SDC and horizontal sync to the source and gate drivers respectively).

Akahori fails to teach wherein the serial protocol image display signal is at least one of red or green or blue pair signal.

The examiner takes official notice that it is well known in the art at the time of the invention that display data signals can include red green and blue pair signals. It would have been obvious to one of ordinary skill in the art at the time of the invention to add

red green and blue pair data to the gray data signal of Akahori in order to allow for a full color display.

Regarding **Claim 18**, Akahori teaches a serial protocol panel display method, comprising:

receiving an image control signal and a clock signal (Akahori, Fig. 1 element 103 receives all signals);

encoding the image control signal into a serial protocol image display signal, according to a serial protocol (Akahori, Fig. 1 element 103 splits the signal into discrete pieces of SDC and horizontal sync);

sequentially transmitting the serial protocol image display signal and the clock signal to a plurality of source drivers (Akahori, Fig. 1 transmits to driver IC, first set of source drivers such as 1001 to 100i);

sequentially transmitting at least a portion of the serial protocol image display signal and the clock signal to a plurality of gate drivers (Akahori, Fig. 1 transmits SDC to driver IC, second set of source drivers such as the drivers 100i+1 to 100n);

decoding the serial protocol image display signal into a first set of control signals and a image information in each of the source drivers, used for pixel display (Akahori, Fig. 10 decodes and outputs image signals to the LCD for first set of drivers);

decoding the serial protocol image display signal into a second set of control signals in each of the gate drivers (Akahori, Fig. 10 decodes and outputs image signals to the LCD for second set of drivers); and

driving the corresponding pixels, according to the first set of control signals, the second set of control signals, and the image information (Akahori, Fig. 1 using the decoded signals to drive the LCD 100).

Akahori fails to teach color information and wherein the serial protocol image display signal is at least one of red or green or blue pair signal.

The examiner takes official notice that it is well known in the art at the time of the invention that display data signals can include red green and blue pair signals which are color signals. It would have been obvious to one of ordinary skill in the art at the time of the invention to add red green and blue pair data to the gray data signal of Akahori in order to allow for a full color display.

Claims 9-11 and 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akahori (US 20050012705) in view of Jun (US 6,300,928).

Regarding **Claim 9 and 27**, Akahori fails to teach a gate driver as claimed. Jun teaches each of the gate drivers includes:

a gate input interface, receiving at least a portion of the serial protocol image signal exported from a VGA unit (Jun, Fig. 1 paragraphs [0011-0013]) and a clock signal (Jun, Fig. 1), wherein the serial protocol image display signal and the clock signal are continuously transmitted to the next one of the gate drivers and are used for decoding out a plurality of gate input signals in the input signals (Jun, Fig. 1, start and clock signals are shifted down the shift register blocks); and

a state in the art gate driver, respectively receiving the gate input signals (Jun, Fig. 1 paragraphs [0011-0013]).

It would have been obvious to one of ordinary skill in the art to use the shift registers as taught by Jun in place of the generic row drivers in Akahori in order to minimizing signal lines (Jun paragraph [0010]).

Regarding **Claims 10 and 28**, Akahori in view of Jun as modified above further teaches that the serial protocol image display signal includes red, green and blue.

Regarding **Claim 11 and 29**, Kim further teaches that the gate input interface includes:

a decoding unit, according to the serial protocol image display signal and the clock signal, decoding into the gate input signals and exporting to the state in the art gate driver (Jun, Fig. 4 the individual shift registers are using the start signal to output to the individual rows); and

a switch unit passing the serial protocol image display signal and the clock signal to the next one of the gate drivers, and coupled with the decoding unit for exporting a clock signal to the state in the art gate driver (Jun, Fig. 4 M6 and r1 and Row1 to the next shift register).

Response to Arguments

Applicant's arguments with respect to claims 1-4, 6-12 and 15-30 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ke Xiao whose telephone number is (571)272-7776. The examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Ke Xiao/
Examiner, Art Unit 2629